# A New Method to Determine the Source Resistance of FET from Measured $S$-Parameters Under Active-Bias Conditions

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*Abstract*— **A new method is proposed to evaluate the source resistance $R_S$ directly from the $S$-parameters of a field-effect transistor biased in the active region. The method is based on the fact that the real part of the feedback admittance is mainly caused by the source and the gate resistance. This enables the analytical calculation of $R_S$ at any measured frequency with high accuracy. Taking the ratio of $R_G$ with regard to $R_S$ as the only optimizing parameter, it is possible to calculate quickly an equivalent circuit the elements of which do not depend on starting values. The equivalent circuit fits the measured $S$-parameters very well and allows a physical interpretation of the calculated elements. By application of the new method in accordance with theoretical considerations one can observe for the first time from rf-measurements a bias-dependence of the source resistance that has been assumed to be constant up to now.**

## I. Introduction

MODELLING the small-signal characteristics of field-effect transistors, equivalent circuits are used which describe the frequency dependence of the device under test accurately. For applications in network simulation the conformity between measured and calculated $S$-parameters is improved by adding more and more elements into the equivalent circuit. This can be used to interpolate or to extrapolate the measurement results. In the latter case, one has to take care that the device is sufficiently small compared with the extrapolated wave length in order to neglect line effects.

On the other hand, an equivalent circuit allows a close view inside the physical structure by observing a bias or temperature dependence of its elements. In this case, it is necessary to create a minimum system which describes the transistor with the fewest possible number of lumped elements. This physical equivalent circuit allows localization of parasitic effects in the device and establishes a feedback for process optimization.

Fig. 1 shows the commonly used equivalent circuit, which describes a field-effect transistor in the saturation range. The capacitances $C_i$ and $C_o$ combined with the inductances $L_G$, $L_D$, and $L_S$ as well as the parasitic resistances $R_G$, $R_D$ and $R_S$ form the extrinsic equivalent circuit, all other elements model the intrinsic FET.

The exact knowledge of the parasitic extrinsic resistances, especially of $R_S$ with its current-voltage feedback effect but also of $R_G$, is important for the accuracy of the whole equivalent circuit because the calculated values of the intrinsic equivalent circuit depend on them.

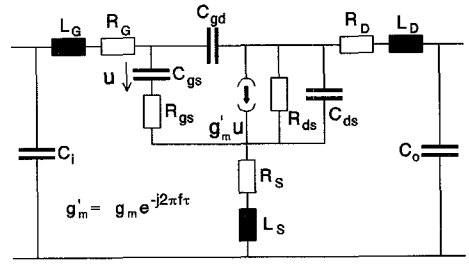


Fig. 1. Commonly used equivalent circuit of a FET under active-bias conditions.

In modern FET structures with short gate lengths below 1 $\mu$m and improved charge control due to gate recess, these parasitic resistances cause the main limitation of performance.

In addition, the bias dependence of the equivalent circuit has to be considered: While all elements of the intrinsic equivalent circuit with the exception of $C_{ds}$ show a clear dependence on dc-bias, many authors postulate the extrinsic elements to be bias-invariant. This assumption must be examined carefully: The inductances and the extrinsic capacitances can be taken as both, bias-independent and identical for all transistors manufactured with the same mask layout, because they model the influence of passive lead to the intrinsic FET.

Although $R_G$ normally should be bias independent too, special device designs with an additional p-acceptor layer for barrier enhancement on n-InP may cause a variation of $R_G$ with bias [5]. However, the assumption of bias independence is not justified for the parasitic resistances $R_D$ and $R_S$. The source and drain resistances consist of three parts: The first and the second part describe the resistances between the calibration plain and the device as well as the contact resistance and may be assumed to be constant, too. The third part, however, describes the resistance between the source or drain contact at the one side and the beginning of the space charge region below the gate at the other side which changes with dc-bias due to the two-dimensional charge control.

The precise knowledge of the bias-dependence of the intrinsic FET as well as of $R_G$, $R_D$, and $R_S$ gives a better insight into the device and enables a further improvement of the technological process. Before presenting the new method to determine the source resistance accurately, it will be briefly discussed in the following section to what extend commonly used extraction methods are able to generate a physically meaningful equivalent circuit.

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## II. Discussion of Existing Equivalent Circuit Extraction Methods

Many commercial CAD programs for circuit evaluation and design use the well known method of multi-dimensional optimization, based on numerical mathematics: By changing all elements of an assumed equivalent circuit, it is possible to minimize an error function which describes the deviation between measured and calculated $S$-parameters [1].

Employing this method only the $S$-parameters under active bias conditions have to be known and the calculated equivalent circuit may fit the measured data quite well. On principle, however, this method is not appropriate to determine a physically meaningful equivalent circuit: The great number of variable elements produces an equivalent circuit strongly depending on the starting values. Especially the extrinsic resistances $R_G$, $R_D$ and $R_S$ vary up to 100% and more, because inaccurately determined values of these quantities can be compensated up to a certain degree by an appropriate choice of the intrinsic elements, mainly of $R_{gs}$ and $g_m$. Due to this effect, the optimizing procedure runs into a local minimum and thus creates an incorrect equivalent circuit —not allowing a physical interpretation of its elements. In addition, the frequency range used to calculate the error function strongly affects the results and last but not least the algorithms consume much computing time.

Therefore, Kondoh introduced the so-called 'step-method' [2]. He examined the influence of the single elements over the four $S$-parameters separately and used eight optimizing cycles successively with different error functions and up to three simultaneously floating equivalent circuit elements. By means of this method the computing time and the possibility that the error function does not converge could be reduced significantly. But only the intrinsic elements $g_m$, $C_{gs}$ and $R_{ds}$ showing the greatest influence on the $S$-parameters can be determined with sufficient accuracy, the strong dependence on the starting values concerning all other elements is not reduced decisively.

In 1988 Dambrine *et al.* [3] pointed out that the circuit topology of the intrinsic FET biased in the saturation range directly represents the $Y$-parameters. This allows the analytical calculation of the intrinsic elements at any single measured frequency if the extrinsic elements have already been determined. Fig. 2 shows the assignment of the elements of the intrinsic FET to the $Y$-parameters. Generally the calculation from measured $S$-parameters yields a complex feed-back admittance between gate and drain with a nonvanishing real part. An additional resistance $R_{gd}$ in series with $C_{gd}$ therefore appears in some publications although it only must be considered in a nonsaturated FET at low drain-source voltages where $C_{gd}$ becomes comparable to $C_{gs}$ according to [4].

The possibility of a direct and fast calculation of the intrinsic elements of the equivalent circuit offers the great advantage that no starting values need to be known. In addition, the frequency dependence of the intrinsic elements can be used to judge the quality of the calculated equivalent circuit: Although the agreement between measured and calculated $S$-parameters can be good, some elements, especially Rgs, may show a great

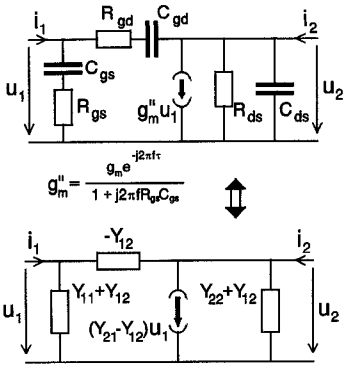


Fig. 2. Attachment of the intrinsic equivalent circuit elements to the intrinsic $Y$-parameters. The transconductance $g''_m$ shows a first-order low-pass behavior due to $R_{gs}$ and $C_{gs}$ combined with a time delay due to $\tau$.

variance, because their influence on the four-pole parameters is small. On the other hand, a steep but smooth gradient of the intrinsic elements over the frequency range is caused by inaccuracies concerning the extrinsic elements as long as the topology of Fig. 1 describes the FET correctly. From this, one can conclude that the main problem remains the determination of the extrinsic elements. An optimizing process yields unsatisfactory results, since the small effects of the parasitics on the $S$-parameters cannot be attributed clearly to various lumped elements.

Therefore, to determine the parasitic resistances, usually dc or low frequency measurements with forward biased gate-source diode are performed [6], [7]. But these measurements are based on a simplified, one-dimensional model, assuming symmetry and homogeneity of the gate-source region. Besides, the operating point is different from that under normal bias conditions and may cause a change of $R_S$ and $R_D$ due to the missing space charge region. Moreover, it is not possible to extract from dc-measurements $R_G$ which models the resistivity per unit length of the gate transmission line. Another disadvantage of this method is the necessity to perform both, dc- and rf-measurements because this requires additional effort at different test desks. As an alternative, the extrinsic elements can be determined by rf-measurements at $U_{ds} = 0$ V and $U_{gs}$ below the pinchoff voltage $U_P$ as well as with a forward biased gate-source diode [1]. In addition rf-measurements at dummy structures without an active device can be performed to determine $R_G$, the extrinsic capacitances and the inductances, employing a simplified equivalent circuit [4].

To summarize, with these methods, the determination of the parasitic resistances remains difficult, inaccurate and time-consuming, and a bias dependence cannot be observed, although theoretical considerations prove the existence of these dependencies [8]–[10].

## III. The New Method for the Calculation of $R_S$ from Measured $S$-Parameters in the Saturation Range

The method proposed here is based on the fact that the real part of the feedback admittance is mainly caused by the source and the gate resistance if the transistor is biased in the saturation regime. This enables the analytical calculation of $R_S$ from four complex measured $S$-parameters at any single frequency.

For this purpose first a relation is deduced from Fig. 2 with $R_{gd} = 0$ between the intrinsic $Y$-parameters and the elements of the intrinsic equivalent circuit according to [3]:

$$(Y_{intr})_{11} = \frac{j\omega C_{gs}}{1 + j\omega R_{gs} C_{gs}} + j\omega C_{gd} \approx \omega^2 R_{gs} C_{gs}^2 + j\omega(C_{gs} + C_{gd}) \quad (1)$$

$$(Y_{intr})_{12} = -j\omega C_{gd} \quad (2)$$

$$(Y_{intr})_{21} = \frac{g_m e^{-j\omega t}}{1 + j\omega R_{gs} C_{gs}} - j\omega C_{gd} \approx g_m - j\omega[g_m(\tau + R_{gs} C_{gs}) + C_{gd}] \quad (3)$$

$$(Y_{intr})_{22} = G_{ds} + j\omega(C_{ds} + C_{gd}). \quad (4)$$

Because of the small time constants $R_{gs}C_{gs}$ and $\tau$ of only a few picoseconds in modern devices, the approximations in (1) and (3) are justified. As an example a typical time constant of 1ps results in an error of about 3% at a frequency of 26.5 GHz which may be an acceptable accuracy of the equivalent circuit elements.

Using the approximation the real part can be clearly separated from the imaginary part of the intrinsic $Y$-parameters:

$$Y_{intr} = G + j\omega C \quad (5)$$

with the matrix symbols $C$ and $G$ defined as:

$$C \triangleq \begin{pmatrix} C_{gs} + C_{gd} & -C_{gd} \\ -g_m(R_{gs}C_{gs} + \tau) - C_{gd} & C_{ds} + C_{gd} \end{pmatrix} \quad (6)$$

$$G \triangleq \begin{pmatrix} \omega^2 C_{gs}^2 R_{gs} & 0 \\ g_m & G_{ds} \end{pmatrix}. \quad (7)$$

It should be emphasized that the simplification by neglecting the higher-order terms in $C$ and $G$ is neither necessary for the evaluation of the intrinsic equivalent circuit nor for the determination of the source resistance which can exactly be calculated at higher frequencies, too. However, an important assumption is made employing the new method: the feedback of the intrinsic FET is purely capacitive. Thus the $(G)_{12}$ component may be neglected and the real part of the feedback admittance is caused mainly by $R_S$ and $R_G$. As shown in Appendix I this condition is not only fulfilled if $(G)_{12} = 0$, but always if $R_S C_{ds} C_{gs} \gg R_{gd} C_{gd}^2$ or $R_G C_{gs} \gg R_{gd} C_{gd}$ can be assumed, which is not critical since $C_{gs}$ is much higher than $C_{gd}$ in the saturation range and a possibly existing $R_{gd}$ should be very small.

For further calculation, the intrinsic $Y$-parameters will be combined with the parasitic resistances $R_G$, $R_D$ and $R_S$ forming the matrix $Y$ ($E \triangleq$ unit matrix):

$$Y = (R + Y_{intr}^{-1})^{-1} \quad (8)$$

$$\Rightarrow \quad Y_{intr} = (Y_{intr} R + E) Y \quad (9)$$

with:

$$R \triangleq \begin{pmatrix} R_S + R_G & R_S \\ R_S & R_S + R_D \end{pmatrix}. \quad (10)$$

On the other hand, the matrix Y can be evaluated from the extrinsic $Y$-parameters $Y_{extr}$ which can be deduced from the measured $S$-parameters using well-known transformation equations. By simple matrix conversion [3], $Y$ can be expressed by the extrinsic inductances and capacitances in the following manner

$$Y = [(Y_{extr} - \omega C_{ex})^{-1} - \omega L]^{-1} \quad (11)$$

with

$$L \triangleq \begin{pmatrix} L_S + L_G & L_S \\ L_S & L_S + L_D \end{pmatrix} \quad (12)$$

$$C_{ex} \triangleq \begin{pmatrix} C_i & 0 \\ 0 & C_o \end{pmatrix}. \quad (13)$$

To continue the calculation of $R_S$ the matrix $Y$ is assumed to be known. By splitting $Y$ in its real and imaginary part $Y = Y_r + jY_i$ and by using (5) and (9), two real matrix equations are obtained which describe the intrinsic transistor combined with the parasitic resistances $R_G$, $R_D$ and $R_S$ completely:

$$G + \omega C R Y_i - G R Y_r = Y_r \quad (14)$$

$$\omega C - \omega C R Y_r - G R Y_i = Y_i. \quad (15)$$

The two matrices (14) and (15) yield a set of nonlinear equations of order eight, from which eight independent variables can be calculated. To solve for $R_S$, the matrix of the extrinsic resistances is rearranged as follows:

$$R = R_S \cdot A = R_S \cdot \begin{pmatrix} \alpha_1 & 1 \\ 1 & \alpha_2 \end{pmatrix} \quad (16)$$

with

$$\alpha_1 \triangleq 1 + \frac{R_G}{R_S} \quad (16a)$$

$$\alpha_2 \triangleq 1 + \frac{R_D}{R_S}. \quad (16b)$$

The new parameters $\alpha_1$ and $\alpha_2$ specify the ratio of the parasitic resistances $R_G$ and $R_D$ with regard to $R_S$ respectively and will be treated as known in the following calculation. Especially the assumption $\alpha_2 = 2$ ($R_D = R_S$) is justified because of the usually small difference between $R_D$ and $R_S$. It will be shown that a deviation of $\alpha_2$ from the value two has only a small influence on the calculated source resistance. However, $\alpha_1$ shows a great effect on the resulting $R_S$ and therefore must be determined accurately. This can be performed by two different methods alternatively, that will be discussed later.

The calculation of $R_S$ results from inserting (16) into (14) and (15). The conversion of the result yields a matrix equation including $R_S$ implicitly

$$GX = N \quad (17)$$

with

$$X \triangleq R_S A(Y_r Y_i^{-1} Y_r + Y_i) + \frac{1}{R_S} Y_i^{-1} A^{-1} - (A Y_r Y_i^{-1} A^{-1} + Y_i^{-1} Y_r) \quad (17a)$$

$$N \triangleq \frac{1}{R_S} Y_r Y_i^{-1} A^{-1} - (Y_r Y_i^{-1} Y_r + Y_i). \quad (17b)$$

First an approximate solution for $R_S$ is considered, which represents the exact solution only if the real part of the intrinsic gate source admittance $(G)_{11}$ can be neglected due to the small time constant $R_{gs}C_{gs}$. In this case, using (17), a one-dimensional linear equation of $R_S$ can be derived with the $(N)_{11}$ component set to zero

$$(N)_{11} = (G)_{11}(X)_{11} + (G)_{12}(X)_{21} = \omega^2 C_{gs}^2 R_{gs} (X)_{11} \approx 0. \quad (18)$$

Then $R_S$ can be evaluated as a function of the matrices $Y$ and $A$ as follows

$$R_S \approx \frac{(Y_r Y_i^{-1} A^{-1})_{11}}{(Y_r Y_i^{-1} Y_r + Y_i)_{11}}. \tag{19}$$

This result yields a simplified but rather exact solution for $R_S$ and beyond enables to estimate the effect of the parameters $\alpha_1$ and $\alpha_2$ on the source resistance (see Appendix B).

For an exact evaluation of $R_S$, it is not necessary to use (19). Considering only the first row of (17) one can deduce another one-dimensional equation that implicitly contains $R_S$:

$$(N)_{11}(X)_{12} = (N)_{12}(X)_{11}. \tag{20}$$

This equation yields a third-order polynom for $R_S$ and can be solved analytically at any frequency by using the Cardanian formula, see Appendix C. Some parameters and frequencies may result in three real solutions, but only one of these solutions is physically meaningful, since the others are much to high or negative. Therefore, the smallest positive solution yields the source resistance showing only a small deviation from the value calculated with (19) due to $R_{gs}$. As an additional proof for the right choice of $R_S$, it may be compared with a single-valued solution at an adjacent frequency leading to an uniquely determined source resistance over the whole measurement range.

## IV. Determination of the Equivalent Circuit by Means of the New Method

By using coplanar on-wafer probe heads it is possible to measure $S$-parameters with sufficient accuracy to determine exactly the elements of the equivalent circuit.

The extrinsic capacitances and the inductances can be extracted as described before. Actually, they just have a small effect on the FET small-signal behavior and on the calculated $R_S$. Moreover, it turns out that the extrinsic elements depend as well on the calibration of the network analyzer as partly on the position of the probe heads on the device. Therefore they should be considered mainly as correction parameters and should not be overinterpreted physically.

Now, with the known matrices $L$ and $C_{ex}$ the matrix $Y$ can be evaluated and split into real and imaginary parts $Y_r$ and $Y_i$. Then after having calculated $R_S$ from (20) at all frequencies, the intrinsic equivalent circuit can be determined by application of (1)–(4), (8), and (16) according to [3].

By means of this new method, it is possible to calculate all the intrinsic elements including $R_S$ and $R_G$ at any frequency dependent just on $\alpha_1$. Since the correct $\alpha_1$-value is not known *a priori*, an optimizing process with $\alpha_1$ as single-variable parameter is performed. During optimization the variance of the deviation between measured and calculated $Y$-parameters is taken as error function, since the $Y$-parameters can be calculated directly from the equivalent circuit without many time consuming transformations, which must be performed only once with the measured $S$-parameters. The lumped elements of the equivalent circuit will be attached by using the median of all calculated values over frequency. This can prove to be more stable against measurement errors than the mean value.

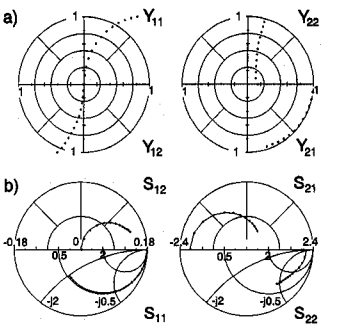


Fig. 3. Measured normalized (a) $Y$- and (b) $S$-parameters (dotted line) as well as $S$-parameters calculated from the equivalent circuit (solid line). The smooth $Y$-parameter curves prove high measurement accuracy and show clearly the effect of the extrinsic resistances.

Another advantage of choosing the $Y$-parameters is shown by the graph in the complex plane: The equidistant points of the $Y$-parameters in Fig. 3(a) ($\Delta f \approx 2$ GHz) permit a uniform weighing over the entire frequency range and show clearly the effect of the parasitic elements, because the variations of the real parts of $Y_{12}$ and $Y_{22}$ with frequency are caused by the extrinsic elements only.

Comparing the proposed direct calculation of $R_S$ with a conventional straightforward optimization of $R_S$ and $R_G$, two main advantages of the new method become obvious:

1) First, the number of optimizing parameters is reduced by 50%: Instead of a two-dimensional approach now just $\alpha_1$ has to be adapted until the error minimum is reached. By varying $\alpha_1$, its crucial influence on the quality of the agreement between measured and calculated parameters is recognized. Therefore the optimization converges rapidly in a few seconds for all starting positions and the problem of running into a local minimum is eliminated. Besides, it is advantageous for the convergence that the lower limit of $\alpha_1$ is the value one ($R_G = 0$) and that the total value range of $\alpha_1$ is quite small for any device because of its definition as a ratio.
2) Second, if the gate resistance of the FET under test has already been determined and can be assumed to be bias-invariant, then it will be possible to calculate $R_S$ without using the error function between the measured and the calculated $Y$-parameters. In this case merely $\alpha_1$ has to be adapted until the known $R_G = R_S(\alpha_1 - 1)$ results.

In order to determine the correct value of $R_D$, which in general is not exactly equal to $R_S$, it is possible to optimize $\alpha_2$, too. Surely, one has to consider that the influence of $\alpha_2$ is small compared to that of $\alpha_1$ and $\alpha_2$ should therefore be varied only if $\alpha_1$ has already been determined.

## V. Results

To test the new method, $S$-parameter measurements of many MESFET and HFET manufactured in our institute have been evaluated [5]. All measurements were performed with coplanar probe heads on a network analyzer HP 8510B using the accurate LRM calibration in the frequency range from 45 MHz to 26.5 GHz. The smooth curves of the $Y$-parameters (Fig. 3(a)) prove the high quality of the measurement, since

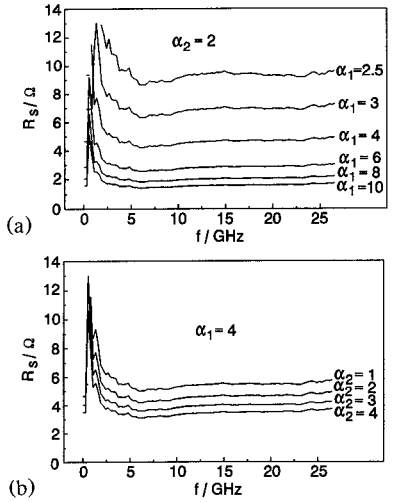


Fig. 4. Effect of (a) $\alpha_1$ and (b) $\alpha_2$ on the calculated source resistance $R_S$; the other $\alpha$-factor has been set to the value 2 and 4, respectively. The strong $\alpha_1$ dependence of $R_S$ becomes obvious while $\alpha_2$ has only little influence.

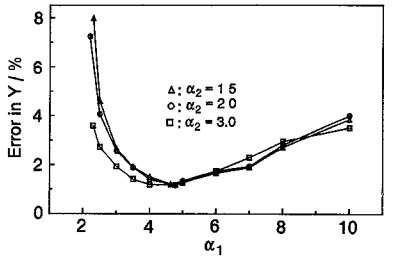


Fig. 5. Error between the measured and calculated $Y$-parameters in percent dependent on $\alpha_1$.

they are derived from the $S$-parameters using a complex transformation, amplifying measurement inaccuracies.

The source resistance of a HFET has been calculated over frequency according to (20). In Fig. 4(a) and (b) the dependence of $R_S$ on $\alpha_1$ and $\alpha_2$ is presented with the other $\alpha$-parameter set to the value two and four, respectively. The results coincide quite well with the behavior expected from (19): $\alpha_2$ has only little influence on the source resistance and therefore it has been set to the fixed value two during optimization of $\alpha_1$ which behaves nearly inversely proportional to $R_S$. From Fig. 4(a) and (b), it can be seen that the source resistance becomes single-valued at frequencies above 5 GHz. At lower frequencies, the resolution of the measurement system is limited due to the very small real part of the feedback admittance which is predominated by a small dc-current.

Although the calculated $R_S$ becomes constant at higher frequencies independent of $\alpha_1$, the resulting error of the $Y$-parameters shows a clear minimum. This is prooved in Fig. 5 where the error of the $Y$-parameters is depicted dependent on $\alpha_1$ with $\alpha_2$ as parameter: It can be seen that the error function has a steep gradient with a single minimum which is reached from any starting position. Since the corresponding $\alpha_{1\,\min}$ does not depend on $\alpha_2$, it is justified to hold this parameter constant during optimization of $\alpha_1$.

The quality of the evaluated equivalent circuit becomes obvious by the small variance of its elements. Fig. 6 shows the calculated intrinsic elements and $R_S$ over the frequency.

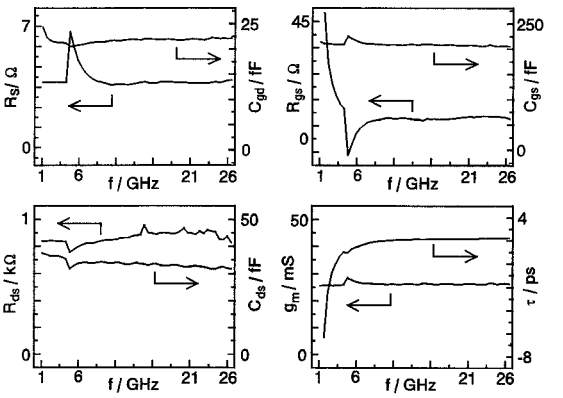


Fig. 6. Frequency dependence of the source resistance and the intrinsic elements ($C_i = C_o = L_S = 0$, $L_G = 13$ pH, $L_D = 8$ pH, $\alpha_2 = 2$). At higher frequencies all elements become single valued which proves the high quality of the calculated equivalent circuit.

To limit the error of the source resistance at low frequencies its calculated value has been replaced by the median, if its deviation to the median exceeds 100%. Since all other intrinsic elements have been calculated with the frequency-dependent value of $R_S$, they show corresponding deviations in the low frequency range. At low frequencies, besides the source resistance also $R_{gs}$ and $\tau$ cannot be calculated definitely, since their influence on the $Y$-parameters is very small. In the higher-frequency range however, a single value can be determined for all elements resulting in good conformity between measured and calculated $S$-parameters (Fig. 3(b)). To test the efficiency of the new method, the dependence of the resulting source resistance on a real existing feedback resistance $R_{gd}$ has been examined. For this purpose, $S$-parameters have been simulated from an equivalent circuit including a feedback resistance $R_{gd} = 10\ \Omega$, which may be an upper limit for $R_{gd}$ since its order of magnitude should be comparable to that of $R_{gs}$. On these $S$-parameters the new method has been applied. The calculated source resistance shows a deviation of only a few percent from the value calculated with $R_{gd} = 0$. From this result, one can conclude that the new method is not sensitive to a real existing intrinsic feedback resistance which allows its application also at the beginning of saturation. Finally, in Fig. 7 the bias-dependences of $R_S$, $g_m$, and $C_{gs}$ are presented which have been calculated just by adapting $\alpha_1$ with $R_G = 14\ \Omega$. If an optimization is performed at every operating point, almost the same values will be obtained. While $g_m$ and $C_{gs}$ show a maximum, a clear decrease of the source resistance $R_S$ with increasing negative gate-source voltage can be observed. This effect can be understood qualitatively, since the lateral extension of the space-charge region will increase with decreasing gate-source voltage. This results in a lower parasitic resistance $R_S$ because of the reduction of the effective gate-source distance.

## VI. Conclusion

Small-signal equivalent circuits yield a close view inside the physical structure of field-effect transistors, localizing parasitic effects and enabling a feedback for device fabrication.

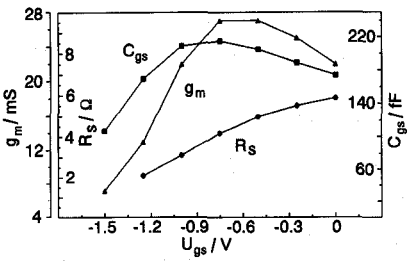


Fig. 7. Gate-source voltage dependence of $R_S$, $g_m$ and $C_{gs}$ for a HFET. While $g_m$ and $C_{gs}$ show a maximum, $R_S$ becomes smaller with increasing negative gate-source voltage.

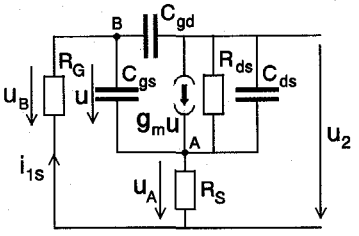


Fig. A1. Equivalent circuit to calculate the real part of $(Y)_{12}$ due to $R_S$ and $R_G$.

A new method to calculate analytically the source resistance $R_S$ at any measured frequency has been proposed, which is based on a single rf-measurement under active-bias conditions.

By means of the new method, it is possible to calculate an accurate equivalent circuit including $R_G$, $R_S$ and $R_D = R_S$ by varying $\alpha_1$, the ratio of $R_G$ to $R_S$, as single optimizing parameter. This results in a very fast convergency of the optimizing algorithm with the calculated equivalent circuit not depending on the starting value of $\alpha_1$.

If the gate resistance $R_G$ is already known and can be assumed to be bias invariant, then alternatively, $R_S$ can be calculated just by adapting $\alpha_1$ without using the error function.

Moreover, the exact value of $R_D$ which only insignificantly influences the four-pole parameters of the FET can be determined by optimizing $\alpha_2$.

By means of the new method one can observe for the first time a bias dependence of $R_S$ and $R_D$ in accordance with theoretical considerations. These results suggest that the commonly used extraction methods can yield only inaccurate values of these parasitics.

## Appendix A
## Effect of $R_S$ and $R_G$ on the Real Part of the Feedback Admittance

To calculate the real part of the feedback admittance $(Y)_{12}$ caused by $R_S$ and $R_G$, the simplified eqivalent circuit in Fig. A1 is used with the input end short circuited according to the definition of $(Y)_{12} = i_{1s}/u_2$. Performing the calculation, it is not necessary to consider the gate-source resistance $R_{gs}$, the phase delay $\tau$ as well as $R_D$ since they do not influence the feedback admittance significantly.

Then utilizing Kirchhoff's first law at the nodes $A$ and $B$ yields two linear equations in dependence on the voltages $u_A$, $u_B$ and $u_2$

$$u_A\left[\frac{1}{R_S}+\frac{1}{R_{ds}}+g_m+j\omega(C_{gs}+C_{ds})\right] - u_B[g_m+j\omega C_{gs}] - u_2\left[\frac{1}{R_{ds}}+j\omega C_{ds}\right]=0 \tag{A1}$$

$$-u_A j\omega C_{gs}+u_B\left[\frac{1}{R_G}+j\omega(C_{gs}+C_{gd})\right] - u_2 j\omega C_{gd}=0. \tag{A2}$$

In (A1) and (A2) the voltage $u$ has been replaced using $u = uB - uA$.

Then, after the elimination of $uA$ and with $uB = -R_G\, i_{1s}$ the complex feedback admittance can be calculated

$$(Y)_{12} \approx \frac{\omega^2 R_S C_{gs}(C_{gd}+C_{ds}) - j\omega C_{gd}}{1+j\omega C_{gs}(R_S+R_G)}. \tag{A3}$$

For simplification of the result, the following approximations have been used in (A3) which are normally well fulfilled for a FET biased in the saturation range $g_m R_S \ll 1$, $C_{gd} \approx C_{ds} \ll C_{gs}$ and $R_S/R_{ds} \ll C_{gd}/C_{gs}$.

Now, the real part of $(Y)_{12}$ can be calculated from (A3) using an expansion in series which is evaluated up to $\omega^2$

$$\mathcal{R}\{(Y)_{12}\} \approx \omega^2 C_{gs}(R_S C_{ds} - R_G C_{gd}). \tag{A4}$$

On the other hand according to Fig. 2 without the parasitic resistances $R_S$, $R_G$ and $R_D$ the real part of the intrinsic feedback admittance $(Y_{intr})_{12}$ is caused by the elements $R_{gd}$ and $C_{gd}$ only and can be calculated as follows:

$$\mathcal{R}\{(Y_{intr})_{12}\} = \mathcal{R}\left\{\frac{-j\omega C_{gd}}{1+j\omega R_{gd}C_{gd}}\right\} \approx -\omega^2 R_{gd} C_{gd}^2. \tag{A5}$$

To compare the influence of $R_S$, $R_G$ and $R_{gd}$ the total differential of the real part of the feedback admittance is considered

$$\delta(Y_r)_{12} = \omega^2(\delta R_S \cdot C_{gs}C_{ds} - \delta R_G \cdot C_{gs}C_{gd} - \delta R_{gd} \cdot C_{gd}^2). \tag{A6}$$

As can be easily seen from (A6) the effect of $R_S$ and $R_G$ on the real part of $(Y)_{12}$ stays significant as long as $R_S C_{ds} C_{gs} \gg R_{gd} C_{gd}^2$ or $R_G C_{gs} \gg R_{gd} C_{gd}$ can be assumed. Since the gate-source capacitance $C_{gs}$ in the saturation range is much higher than $C_{gd}$ and with $C_{ds} \approx C_{gd}$ and $R_G \approx R_S \approx R_{gd}$ these conditions are fulfilled independent of frequency.

## Appendix B
## Effect of $\alpha_1$ and $\alpha_2$ on the Calculated Source Resistance

From (19), the influence of $\alpha_1$ and $\alpha_2$ can be estimated by performing the calculation of the numerator

$$R_S \propto \frac{\alpha_2(Y_r Y_i^{-1})_{11} - (Y_r Y_i^{-1})_{12}}{\alpha_1\alpha_2 - 1} \propto \frac{1-\dfrac{K}{\alpha_2}}{\alpha_1 - \dfrac{1}{\alpha_2}} \tag{B1}$$

with:

$$K = \frac{(Y_r Y_i^{-1})_{12}}{(Y_r Y_i^{-1})_{11}} = \frac{(Y_r)_{12}(Y_i)_{11} - (Y_r)_{11}(Y_i)_{12}}{(Y_r)_{11}(Y_i)_{22} - (Y_r)_{12}(Y_i)_{21}}. \quad \text{(B1a)}$$

The imaginary part of $Y$ is not significantly influenced by the extrinsic resistances, therefore $Y_i \approx \omega C$ can be assumed. Furthermore, the real part of the feedback admittance is determined according to (A4) and the real part of the input admittance $(Y_r)_{11}$ can be simply deduced from the equivalent circuit with $g_m R_S \ll 1$ as follows:

$$(Y_r)_{11} \approx \omega^2 C_{gs}^2 (R_{gs} + R_G + R_S). \quad \text{(B2)}$$

Then the constant $K$ can be calculated using that $C_{gd}$, $C_{ds} \ll C_{gs}$ in the saturation range and with $(C)_{21} \approx (C)_{22}$ in the following manner:

$$K \approx 1 - \frac{1}{\left(1 + \frac{C_{gd}}{C_{ds}}\right)\left(1 + \frac{R_S}{R_{gs} + R_G}\right)} < 1. \quad \text{(B3)}$$

With typical values for the elements in (B3) the constant $K$ becomes smaller than 0.5 . Since $\alpha_2 \approx 2$ and $\alpha_1 > 1$ one can exspect from (A6) that the source resistance behaves about inversely proportional to $\alpha_1$ while showing only a small dependence on a variation of $\alpha_2$.

## Appendix C
## Exact Solution for $R_S$ by Using the Cardanian Formula

The calculation of $R_S$ using (20) is straightforward and not difficult but time consuming, therefore the results are presented. First, according to (17a) and (17b) the new matrices $M_1$, $M_2$, $M_3$, and $K_1$, $K_2$ will be defined

$$X = R_S M_1 + \frac{1}{R_S} M_2 - M_3 \quad \text{(C1a)}$$

$$N = \frac{1}{R_S} K_1 - K_2. \quad \text{(C1b)}$$

Then the coefficients in the cubic polynom $aR_S^3 + bR_S^2 + cR_S + d = 0$ are determined as follows:

$$a = (K_2)_{12}(M_1)_{11} - (K_2)_{11}(M_1)_{12} \quad \text{(C2a)}$$

$$b = (K_1)_{11}(M_1)_{12} - (K_1)_{12}(M_1)_{11} + (K_2)_{11}(M_3)_{12} - (K_2)_{12}(M_3)_{11} \quad \text{(C2b)}$$

$$c = (K_1)_{12}(M_3)_{11} - (K_1)_{11}(M_3)_{12} + (K_2)_{12}(M_2)_{11} - (K_2)_{11}(M_2)_{12} \quad \text{(C2c)}$$

$$d = (K_1)_{11}(M_2)_{12} - (K_1)_{12}(M_2)_{11}. \quad \text{(C2d)}$$

Now the cardanian formula with

$$p = \frac{c}{a} - \frac{b^2}{3a^2} \quad \text{(C3a)}$$

$$q = \frac{2b^3}{27a^3} - \frac{bc}{3a^2} + \frac{d}{a} \quad \text{(C3b)}$$

$$u = \sqrt[3]{-\frac{q}{2} + \sqrt{D}} \quad \text{(C4a)}$$

$$v = \sqrt[3]{-\frac{q}{2} - \sqrt{D}} \quad \text{(C4b)}$$

$$D = (p/3)^3 + (q/2)^2 \quad \text{(C4c)}$$

yields one real solution for $R_S$ if $D > 0$. Generally with $D \leq 0$ three real solutions of the cubic polynom may exist yet only one of them is physically meaningful:

$$R_{S1} = u + v - \frac{b}{3a} \quad \text{(C5a)}$$

$$R_{S2} = -\frac{u+v}{2} + j\sqrt{3}\frac{u-v}{2} - \frac{b}{3a} \quad \text{(C5b)}$$

$$R_{S3} = -\frac{u+v}{2} - j\sqrt{3}\frac{u-v}{2} - \frac{b}{3a}. \quad \text{(C5c)}$$

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